REMARKS/ARGUMENTS

In the Office Action mailed June 26, 2008, claims 1 and 3 – 8 were rejected and claims 9 – 13 are allowed. Applicants hereby request reconsideration of the application in view of the below-provided remarks.

For reference, the formatting of the claims has been changed to show the subscripts and the equations as provided in the corresponding PCT application (PCT/IB04/51894, WO 2005/034358). No substantive changes have been made to the claims.

Allowable Subject Matter

Applicants appreciate the Examiner's review of and determination that claims 9 – 13 are allowable and the determination that claims 1 and 3 – 8 would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. 112, second paragraph, as set forth below.

Claim Rejections under 35 U.S.C. 112

Claims 1 and 3 – 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office action states that claim 1 is indefinite because:

> "it is not clear to the examiner how the logic works. What is being NANDed with what? It appears that the ANDed outputs are being ORed together, is this accurate? It is requested that applicant provide a diagram showing the logic gates with inputs corresponding to the equation. It may help to clear up the examiner's confusion." (Office action, page 2)

Applicants respectfully assert that claim 1, as written, particularly points out and distinctly claims the subject matter which Applicants regard as the invention. However, in order to clear up any confusion that may exist with the Examiner, Applicants point out that Fig. 4 of the specification shows a circuit diagram of a phase selective unit (PSU).

The circuit of this circuit diagram is a particular implementation to generate the output OUT of the phase selection unit of the logic code:

$$OUT = \overline{NC0 \bullet NC1 \bullet INi} + \overline{NC0 \bullet C1 \bullet INni} + \overline{C0 \bullet NC2 \bullet INnq} + \overline{CO \bullet C2 \bullet INq},$$

wherein,

$+, \bullet, \overline{\ }$ represent an OR-, AND, and NAND functions, respectively.

Within paragraphs [0044] and [0045] of Applicants' specification (as published, US 2006/0290433 A1), the circuit design is specified as:

> "[0044] The above logic code comprises four branches which are OR-connected. The first branch is realized by the transistors T1, T9 and T17. The second is implemented by the transistors T1, T11 and T18. The third branch is implemented by transistors T3, T13 and T19. The fourth branch is implemented by transistors T3, T15 and T20.
>
> [0045] The AND logic function, e.g. the first branch $NC0 \bullet NC1 \bullet INi$, is implemented differentially by current switching. The NAND logic is implemented by differentially switching the inputs in the current domain. The OR logic is implemented by adding the output current of the NAND logic in the loads R."

Additionally, Applicants provide herewith a marked up copy of Fig. 4, which is marked up to illustrate the four branches representing the four AND logic functions: $NC0 \bullet NC1 \bullet INi$, $NC0 \bullet C1 \bullet INni$, $C0 \bullet NC2 \bullet INnq$ and $C0 \bullet C2 \bullet INq$. In particular, marked up Fig. 4 illustrates branch 1 (including T1, T9, and T17), branch 2 (including T1, T11, and T18), branch 3 (including T3, T13, and T19), and branch 4 (including T3, T15, and T20). By differentially switching the inputs (INi, INni, INnq, INq), the corresponding NAND logic functions, e.g., $\overline{NC0 \bullet NC1 \bullet INi}$ are implemented. The OR logic connecting these NAND logic functions is implemented by adding the output current of these NAND logic functions in the loads R. Applicants respectfully hope that above-provided discussion has cleared up any confusion that may have existed with the Examiner.

Accordingly, Applicants respectfully request that the rejection of claims 1 and 3 – 8 under 35 U.S.C. 112, second paragraph, be withdrawn.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

Petition is hereby made under 37 CFR 1.136(a) to extend the time for response to the Office Action of 09/26/2008 to and through 11/26/2008, comprising an extension of the shortened statutory period of two months.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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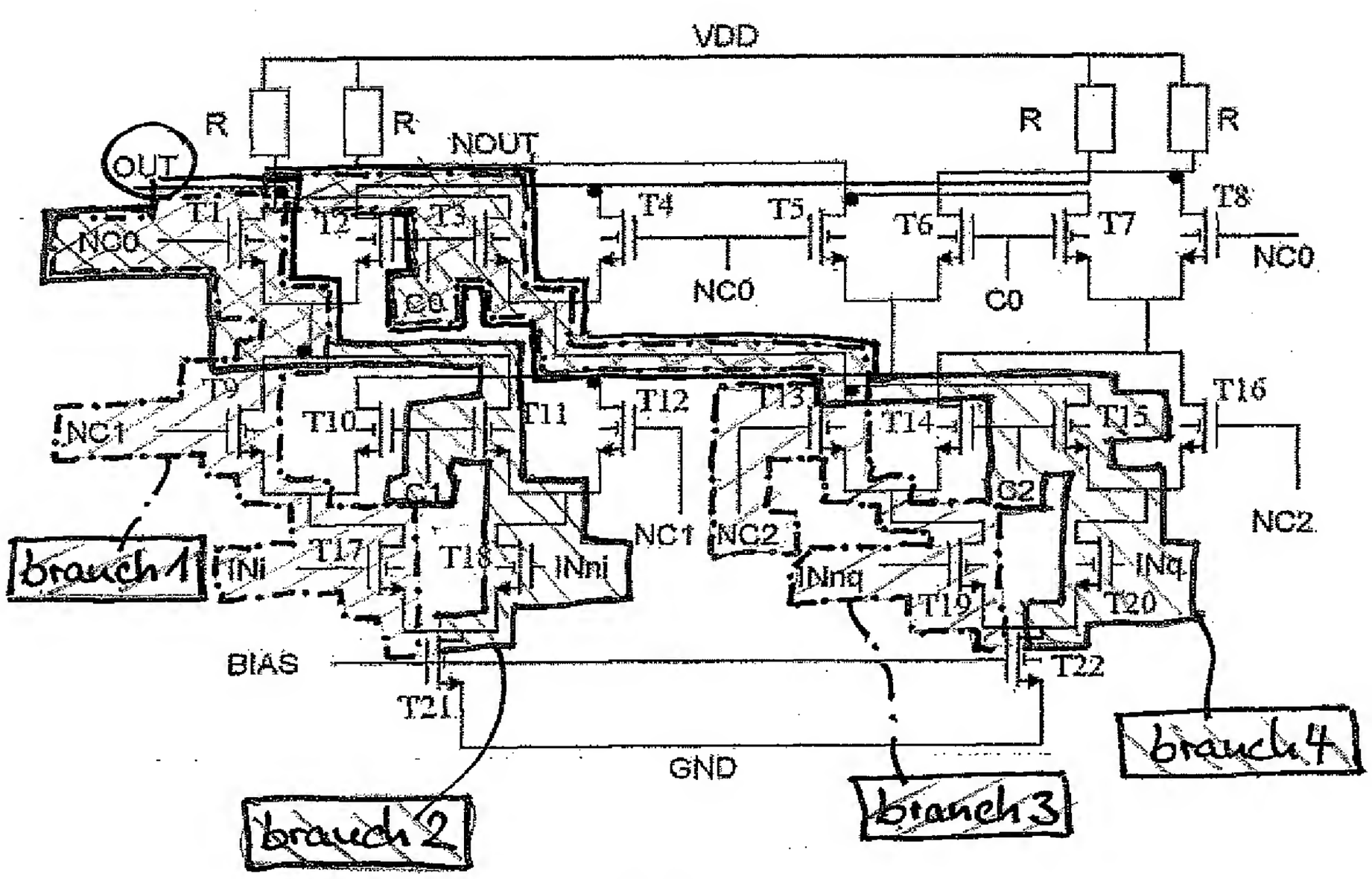
VDD
R
R
R
R
OUT
NOUT
T1
T2
T3
T4
T5
T6
T7
T8
NC0
C0
NC0
C0
NC0
T9
T10
T11
T12
T13
T14
T15
T16
NC1
C1
C2
NC2
NC1
NC2
branch1
INi
T17
T18
INni
INnq
INq
T19
T20
BIAS
T22
T21
GND
branch2
branch3
branch4

FIG.4